ABSTRACT

A method of forming shallow trench isolation using CMP is described. A pad oxide layer is grown overlying a silicon semiconductor substrate. A polysilicon layer is deposited overlying the pad oxide layer. A nitride layer is deposited overlying the polysilicon layer. Trenches are etched through the nitride layer, polysilicon layer, and pad oxide layer into the silicon semiconductor substrate and filled with an oxide layer. In one alternative, a silicon oxynitride layer is deposited overlying the oxide layer. A first polishing is performed to polish away the silicon oxynitride layer and oxide layer using a first slurry having high selectivity of oxide to nitride. A second polishing is performed to polish away the oxide layer using a second slurry having a low selectivity of oxide to nitride and having low-defect properties. The nitride layer is removed and a third polishing is performed to planarize the oxide layer using a third slurry having high selectivity of oxide to polysilicon to complete formation of shallow trench isolations. In a second alternative, the oxide layer is etched away except where it overlies the trenches. A first polishing is performed to polish away the oxide layer using a first slurry having a low selectivity of oxide to nitride and having low-defect properties. A second polishing is performed to polish away the oxide layer using a second slurry having high selectivity of oxide to nitride to complete STI formation.